PROPOSED EXAMINER AMENDMENTS

JUNE 21, 2005

1. (Previously Presented) A method of accessing state from a configurable processor, the method comprising:

preparing a first state-accessing instruction stream based on a first user description of the configurable processor;

transmitting, using a debugger, the first state-accessing instruction stream to an interpreting agent, the interpreting agent being capable of interpreting that stream;

causing, using the first state-accessing instruction stream, the interpreting agent to return the state of a first configuration of the configurable processor to the debugger

preparing a second different state-accessing instruction stream based on a second different user description of the configurable processor;

transmitting, using the debugger, the second state-accessing instruction stream to the interpreting agent, the interpreting agent also being capable of interpreting that second stream; and

causing, using the second state-accessing instruction stream, the interpreting agent to return the state of a second different configuration of the configurable processor to the debugger.

2. (Original) A method as in claim 1 where the interpreting agent is a monitor program.

3. (Original) A method as in claim 1 where the interpreting agent is an instruction insertion server.

4. (Original) A method as in claim 1 where the interpreting agent is an architectural simulator.

5. (Previously Presented) A method as in claim 1, wherein the steps of preparing the first and second state-accessing instruction streams include:

reading, using the debugger, information describing the first and second configurable processor's state architecture, respectively; and

generating, using the debugger, the first and second instruction streams, respectively, based on the information.

6. (Original) A method as in claim 5 wherein the interpreting agent is a monitor program.

7. (Original) A method as in claim 5 wherein the interpreting agent is an instruction insertion server.

8. (Original) A method as in claim 5 wherein the interpreting agent is an architectural simulator.

9. **(Currently Amended)** A computer-readable storage medium storing therein a software program comprising:

software for automatically generating a hardware description of a configurable processor from a user description of that processor; and

a debugger library for automatically generating information necessary to describe save and restore instructions for state of the configurable processor based on the user description**; and**

**a debugger which is capable of requesting an interpreting agent to access state from the configurable processor using a state-accessing stream that is based on the user description, the interpreting agent being capable of interpreting the stream and returning the state of the configurable processor in response thereto**.

10. **(Currently Amended)** A computer-readable storage medium **according to claim 9, wherein the** ~~storing therein a~~ debugger library **is further** for:

reading a description of save and restore state information of [[a]] **the** configurable processor; and

generating saving and restoring state instruction streams that are capable of being executed on the configurable processor based on the description.

11. (Previously Presented) A medium as in claim 10 wherein the debugger library further comprises functionality for:

identifying interdependencies in a state that has been added to the configurable processor based on a user description; and

generating a complete and correct save and restore sequence based on the interdependencies.

12. (Previously Presented) An instruction-insertion server comprising:

means for interpreting both first and second different state-accessing instruction streams, the first and second instruction streams being generated based on first and second different user descriptions of a configurable processor, respectively;

means for retrieving system topology information of a chip containing multiple cores from a computer-readable file; and

means for determining where first and second cores corresponding the first and second different user descriptions are in a system described by the file; and

means responsive to the determining means for directing the first and second state-accessing instruction stream to the first and second cores, respectively.

13. (Previously Presented) A system for accessing state from a configurable processor, the system comprising:

a debugger which transmits a state-accessing instruction stream;

an interpreting agent which

receives the instruction stream,

interprets the instruction stream to access state of the configurable processor, and

returns the accessed state of the configurable processor to the debugger,

wherein the interpreting agent is capable of interpreting both first and second ones of the state-accessing instruction streams which access state of first and second different configurations of the configurable processor, respectively, the first and second configurations being generated based on first and second different user descriptions of the configurable processor.

14. (Original) A system as in claim 13 where the interpreting agent is a monitor program.

15. (Original) A system as in claim 13 where the interpreting agent is an instruction insertion server.

16. (Original) A system as in claim 13 where the interpreting agent is an architectural simulator.

17. (Previously Presented) A system as in claim 13, wherein the debugger is adapted to:
read information describing the configurable processor's state architecture; and
generate the instruction stream based on the information.

18. (Original) A system as in claim 17 wherein the interpreting agent is a monitor program.

19. (Original) A system as in claim 17 wherein the interpreting agent is an instruction insertion server.

20. (Original) A system as in claim 17 wherein the interpreting agent is an architectural simulator.